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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/691,852	10/22/2003	Tae Woong Kang	5882P061	6710

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EXAMINER	
RICHARDS, N DREW	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 03/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/691,852	KANG ET AL.	
	Examiner	Art Unit	
	N. Drew Richards	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) *1-3* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4 and 8-10* is/are rejected.

7)☒ Claim(s) *5-7,11,12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/22/03,8/11/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of Group I, claims 4-12, in the reply filed on 12/6/04 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

3. Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

4. The drawings are objected to because figure 2 includes non-English language characters. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

5. Claims 4-6 and 10-12 are objected to because of the following informalities:

a. Claim 4 line 1 should recite "manufacturing **a** single electron device"

b. Claim 4 line 3 should recite "regions of **a** semiconductor layer"

c. Claim 4 line 4 should recite "apart **from** each"

d. Claim 4 line 6 should recite "defining **an** active region"

e. Claim 4 line 13 should recite "active region" instead of "region**s**"

f. Claim 5 lines 1-2 should recite "the step of **changing the amorphous silicon layer into** the hemisphere-type silicon layer comprises **the** steps of:"

g. Claim 5 line 3 should recite "silicon contain**ing**"

h. Claim 6 line 1 should recite "silicon contain**ing**"

i. Claim 10 line 2 should recite "an uppermost" instead of "a most upper"

j. Claim 11 line 9 should recite "apart **from** each other"

k. Claim 11 line 16 should recite "having **a** plurality"

l. Claim 12 line 2 should recite "comprises **the** steps"

Appropriate correction is required.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 4 and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ueda et al. (U.S. Patent No. 6,103,600), in view of Brousseau (U.S. Patent No. 6,673,717 B1).

Ueda et al. teach a method of manufacturing a single electron device on a substrate in figures 1A-16 and columns 1-18. Specifically, Ueda et al. teach on column 2 lines 14-53, for example:

- forming source/drain regions 8, the source region 8 and the drain region 8 being spaced a predetermined distance apart from each other (figure 13A; column 2 lines 25-26 and lines 51-52; the source is region 8 on the left side and the drain is region 8 on the right, corresponding to source terminal 1 and drain terminal 2 in figure 13F);
- defining an active region between the source and drain region by depositing an amorphous silicon layer 9 on the semiconductor substrate (figure 13A; column 2 lines 27-37);
- changing the amorphous silicon layer 9 into a hemisphere-type silicon layer 3 having a plurality of silicon electron islands 3 (figure 13B; column 2 lines 36-38);
- forming a gate insulating layer 10 on the top surface of the entire structure (figure 13B); and
- forming a gate electrode 11 on the gate insulating layer 10 in order to apply voltages to the active region (figure 13C).

Ueda et al. do not teach the source/drain regions 8 being formed of a semiconductor layer. Brousseau teach a single electron transistor and method of manufacturing the same in figures 1A-6 and on columns 1-12. Brousseau teach in figure 1D, for example, a single electron device including source/drain electrodes 110a/110b (first and second electrodes), a nanoparticle 160 (active region) between the source/drain electrodes, and agate electrode 170. See figure 1D and column 7 lines 1-14. Ueda et al. teach their device formed on a substrate 100 that may be formed of

conventional monocrystalline silicon or a semiconductor-on-insulator (SOI) substrates and that the first and second electrodes (source/drain electrodes) may comprise any of the materials of the substrate or other conductive materials such as conductive polysilicon or metal. Thus, Brousseau teach that metals or semiconductors (monocrystalline silicon or polysilicon) can be used for the source/drain electrodes and teaches their equivalence for the known use of a source/drain electrode in a single electron transistor.

At the time of the invention it would have been obvious to one of ordinary skill in the art to use a semiconductor layer (for instance, either the monocrystalline silicon or polysilicon of Brousseau) in place of the metal layer for the source and drain electrodes of Ueda et al. Since metal source/drain regions were art-recognized equivalents at the time of the invention, one of ordinary skill in the art would have found it obvious to substitute a semiconductor layer for the metal source/drain region of Ueda et al.

Further, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416 (CCPA 1960). Also, the use of conventional materials to perform their known functions in a conventional process has been held as being obvious. In re Raner, 134 USPQ 343 (CCPA 1962).

With regard to claims 8 and 9, Ueda et al. do not explicitly recite the dimension of the predetermined distance between the source/drain regions, nor do Ueda et al. explicitly recite the thickness of the hemisphere-type silicon layer and the size of the

electron islands. Nonetheless, it was well known to one of ordinary skill in the art at the time of the invention to reduce device sizes (channel lengths between source/drain regions) to 100 nm or less. It is well established that single electron transistors are formed to these device dimensions. See, for example, Brousseau who teach a "channel length" (pore size) of less than about 20 nm (column 5 lines 16-18 where the spacer [distance between the source and drain] is about 20 nm). It is a well known industry goal to reduce device sizes to allow for faster circuits which consume less power and can be integrated to a greater degree to fit more devices on a smaller area. Thus, it would have been obvious to form the predetermined distance of Ueda et al. to 100 nm or less. With regard to the thickness of the hemisphere-type silicon layer and the size of the electron islands, these two dimensions are key parameters in determining the operating characteristics of the single electron transistor. These parameters may be changed as optimization or design choice to provide advantageous operating characteristics such as threshold voltage.

These claims are prima facie obvious without showing that the claimed ranges achieve unexpected results relative to the prior art range. In re Woodruff, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also In re Huang, 40 USPQ2d 1685, 1688(Fed. Cir. 1996)(claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also In re Boesch, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and In re Aller, 105 USPQ 233

(CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious).

With regard to claim 10, Ueda et al. teaches a silicon wafer 5 with silicon dioxide films 6 and 7 thereon and the single electron transistor formed on silicon dioxide films 6 and 7 (figure 13A-13F). Ueda et al. alone does not teach a "semiconductor-on-insulator" (SOI) substrate where the semiconductor layer is an uppermost layer of the SOI substrate. However, as combined with Brousseau above, the source/drain regions are modified such that they are formed from a semiconductor material (monocrystalline silicon or polysilicon). When the semiconductor source/drain regions of Brousseau are used in the process of Ueda, the result is an SOI substrate where the semiconductor layer is an uppermost layer of the SOI substrate (**S**emiconductor source/drain regions formed **O**n **I**nsulator silicon oxide - SOI). It is noted that the term "semiconductor-on-insulator" has not been specifically defined by applicant in their specification and thus is given its broadest reasonable interpretation.

Allowable Subject Matter

8. Claims 5-7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims as well as to correct any claim objections listed above.

9. Claims 11 and 12 are objected to above but would be allowable if rewritten to correct any claim objections listed above.

10. The following is a statement of reasons for the indication of allowable subject matter: Prior art of record fails to teach, disclose or suggest, either alone or in combination the method as claimed in claims 5 or 11. With regard to claim 5, the prior art of record fails to teach changing the amorphous silicon into a hemisphere-type silicon by spraying a silicon containing gas while maintaining the amorphous silicon layer at a temperature of 500-700 degrees Celsius and a high vacuum state and then performing a heat treatment as recited in claim 5. With regard to claim 11, the prior art fails to teach simultaneously manufacturing a single electron device and a MOS transistor including the step of defining a source and drain region of the single electron device in the A region, the source and the drain region being spaced a predetermined distance apart from each other and simultaneously defining a source, a drain, and an active region of the MOS transistor with one body in the B region.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Sugiyama et al. (US Patent No. 6060743), Grupp (US Patent No. 6198113 B1), Chae et al. (US 2002/0167002 A1), Shih et al. (US Patent No. 6586787 B1), Flagan et al. (US Patent No. 6723606 B2).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (571) 272-1736. The examiner can normally be reached on Monday-Friday 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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